93448
ISOPLANAR SCHOTTKY TTL MEMORY
512×8-BIT PROGRAMMABLE READ ONLY MEMORY

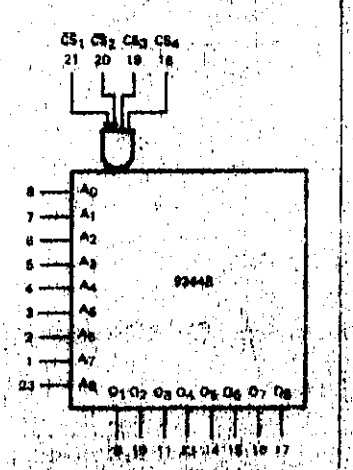
ESCRIPTION – The 93448 is a fully decoded 4096-bit field Programmable ROM organ-d 512 words by eight bits per word. The 93448 has 3-state outputs. The device is abled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93448 is supplied th all bits stored as logic "1"s and may be programmed to logic "0"s by following the ld programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZATION – 512 WORDS X 8 BITS
- 3-STATE OUTPUTS
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 24-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS FOR HIGH RELIABILITY
- REPLACES TWO 256 X 8 PROMs – DOUBLE DENSITY WITH SAME SPACE AND POWER

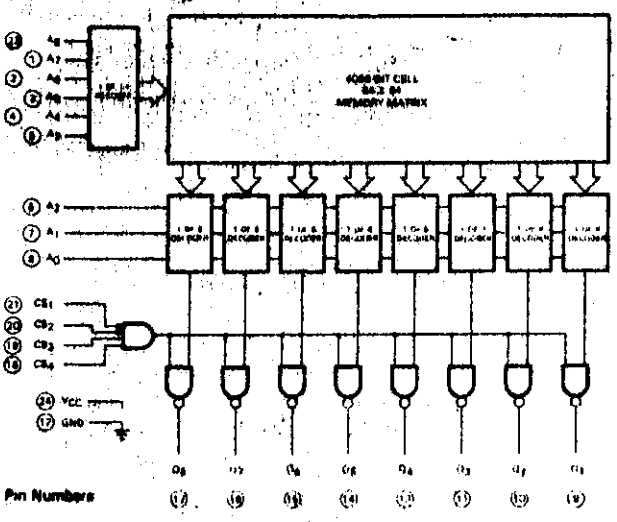
IN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CS}_1, \overline{CS}_2, CS_3, CS_4$	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

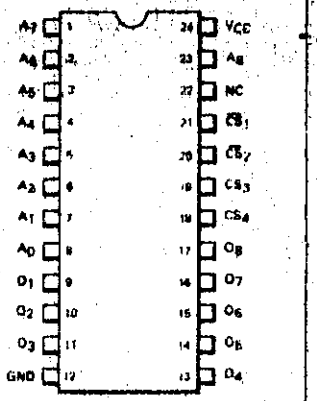


LOGIC DIAGRAM



○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC}	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltages	-0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	AMBIENT TEMPERATURE
93448XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93448XM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

X = package type: F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 93448 is a bipolar field Programmable Read Only Memory (PROM) organized 51[illegible] words by eight bits per word. The 93448 has 3-state outputs which provide active pull-ups when enabled and high outp[illegible] impedance when disabled. Chip Select for both devices follows the logic equation: $\overline{CS}_1 \cdot \overline{CS}_2 \cdot CS_3 \cdot CS_4 = CS$; i.e., if CS[illegible] and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition[illegible] all eight outputs are disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 thro[illegible] A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the procedures in Chapter 6, page 6-[illegible]

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise note.

SYMBOL	CHARACTERISTIC	LIMITS MIN	TYP (Note 1)	MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_0 = +10.8 V, A_1 - A_8 = HIGH
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = -2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State			50 -50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 -50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V -55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All I[illegible]
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All I[illegible]
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		-160 -160	-250 -250	µA µA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			40 40	µA µA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			-1.2	V	V_{CC} = MIN, I_A = -18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

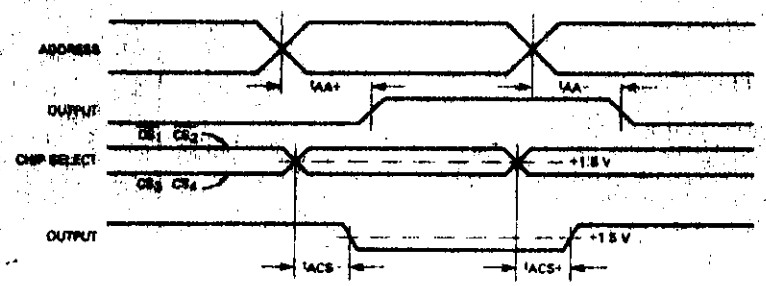
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		35	55	ns	See Waveforms and Test Circuits
t_{AA+}			35	55	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

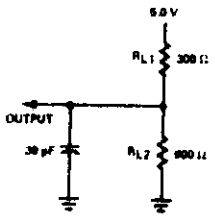
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		35	70	ns	See Waveforms and Test Circuits
t_{AA+}			35	70	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

Note (1): Typical values are at V_{CC} = 5.0 V, 5.0 V, +25°C and max loading.

SWITCHING WAVEFORMS



SWITCHING TEST OUTPUT LOAD



16 mA Load

Fig. 1

93417

ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT PROGRAMMABLE READ ONLY MEMORY

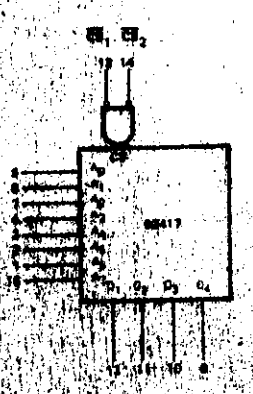
DESCRIPTION — The 93417 is a fully decoded high-speed 1024-bit field Programmable ROM organized 256 words by four bits per word. The 93417 has uncommitted collector outputs. The outputs are disabled when either $\overline{CS}_1$ or $\overline{CS}_2$ are in the HIGH state. The 93417 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZED 256 X 4 BITS PER WORD
- UNCOMMITTED COLLECTORS
- [illegible] ON-CHIP ADDRESS DECODER AND BUFFER
- [illegible] FOR EASY MEMORY EXPANSION
- [illegible]
- [illegible] CODE IN LOW PACKAGE
- [illegible] HIGH RELIABILITY

PIN NAMES

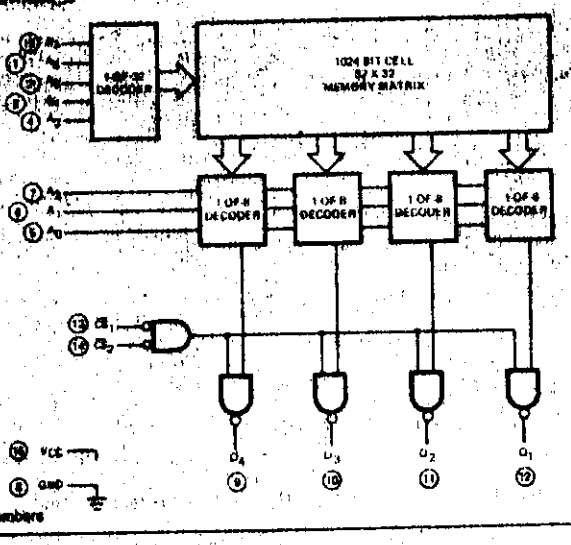
A_0 - A_7	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
O_1 - O_4	Data Outputs

LOGIC SYMBOL

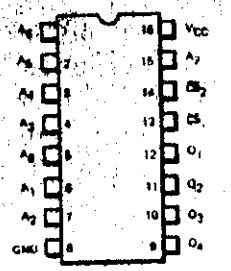


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93417 is a bipolar field Programmable Read Only Memory (PROM) organized 256 words by four bits per word. Open collector outputs are provided for use in wired-OR systems. Chip Selects are active LOW, conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93417 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltage	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	AMBIENT TEMPERATURE
93417PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93417DC	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package type: P for Hermetic, D for Ceramic D.I.P., F for Plastic D.I.P. See Package Information on this page sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted

SYMBOL	CHARACTERISTIC	LIMITS MIN	TYP (Note 1)	MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current			50	µA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		−160 −160	−250 −250	µA µA	V_{CC} = MAX, V_R = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			40 40	µA µA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			-1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

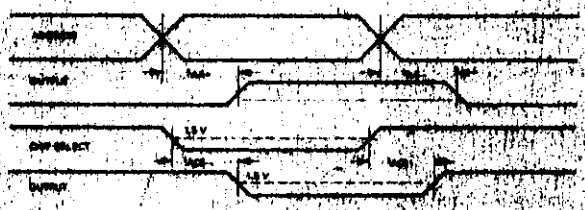
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	45	ns	See Waveforms and Test Circuits
t_{AA+}			26	45	ns	
t_{ACS-}	Chip Select Access Time		12	20	ns	
t_{ACS+}			12	20	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

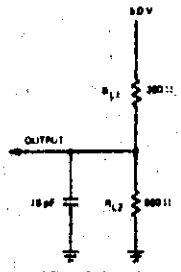
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	60	ns	See Waveforms and Test Circuits
t_{AA+}			26	60	ns	
t_{ACS-}	Chip Select Access Time		12	30	ns	
t_{ACS+}			12	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORMS



AC TEST OUTPUT LOAD



15 mA Load

93427
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT PROGRAMMABLE READ ONLY MEMORY

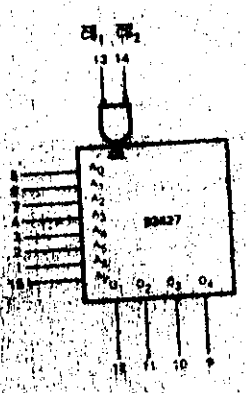
DESCRIPTION - The 93427 is a fully decoded high-speed 1024-bit field Programmable ROM organized 256 words by four bits per word. The 93427 has 3-state outputs. The outputs are disabled when either $\overline{CS}_1$ or $\overline{CS}_2$ are in the HIGH state. The 93427 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZED 256 WORDS BY 4-BITS PER WORD
- 3-STATE OUTPUTS
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- DUAL COMPLEMENTARY INPUTS PROVIDE EASY MEMORY EXPANSION
- [illegible]
- [illegible] DUAL IN-LINE PACKAGE
- [illegible] – FOR HIGH RELIABILITY

PIN NAMES

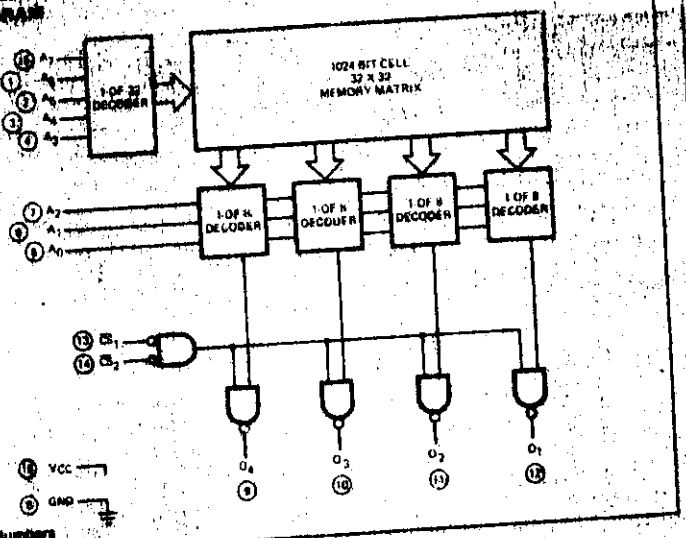
$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
$O_1 - O_4$	Data Outputs

LOGIC SYMBOL

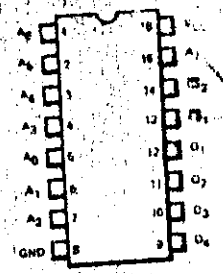


V_{CC} = Pin 15
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93427 is a bipolar field Programmable Read Only Memory (PROM) organized 256 words by four bits per word. The 93427 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93427 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 8, page 8-14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltage	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	AMBIENT TEMPERATURE
93427XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93427XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type: F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information for outline specifications.

DC CHARACTERISTICS over guaranteed operating ranges unless otherwise noted

SYMBOL	CHARACTERISTIC	LIMITS MIN	TYP (Note 1)	MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.5 V, A_1 through A_7 = HIGH	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State			50	µA	V_{OH} = 2.4 V	0°C to +75°C
				−50	µA	V_{OL} = 0.4 V	
I_{off}	Output Leakage Current for HIGH Impedance State			100	µA	V_{OH} = 2.4 V	−55°C to +125°C
				−50	µA	V_{OL} = 0.4 V	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current					V_{CC} = MAX, V_F = 0.45 V	
	I_{FA} (Address Inputs)		−160	−250	µA		
	I_{FCS} (Chip Select Inputs)		−160	−250	µA		
I_R	Input HIGH Current					V_{CC} = MAX, V_R = 2.4 V	
	I_{RA} (Address Inputs)			40	µA		
	I_{RCS} (Chip Select Input)			40	µA		
I_{CC}	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open, Inputs Grounded and Chip Selected	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

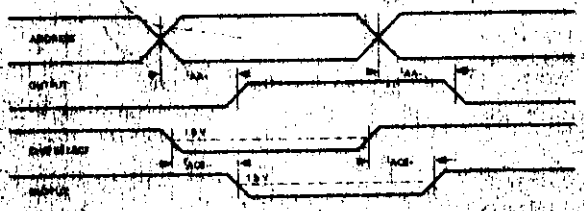
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	45	ns	See Figure 1
t_{AA+}			25	45	ns	
t_{ACS-}	Chip Select Access Time		12	20	ns	
t_{ACS+}			12	20	ns	

AC CHARACTERISTICS: T_A = -55°C to +125°C, V_{CC} = 5.0 V ± 10%.

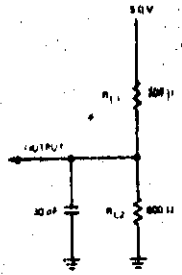
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	60	ns	See Figure 1
t_{AA+}			25	60	ns	
t_{ACS-}	Chip Select Access Time		12	30	ns	
t_{ACS+}			12	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORMS



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1